In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 6, lines 4 to 9 as follows:

--The MDSM system paths, by which the four-way shared dual access RAM data flows, are directed by way of the global traffic modules (global traffic module ~~114~~ 115 in subsystem A 101). Each global traffic module drives a four-way shared DARAM wrapper (DARAM4W 127 in subsystem A 101) that contains the arbitration logic necessary to avoid bus collisions.--

Rewrite the paragraph at page 6, line 10 to page 7, line 8 as follows:

--Figure 2 illustrates in block diagram ~~from~~ form individual functional blocks comprising subsystem A 101. Subsystems B 102, C 103 and D 104 are identical to subsystem A 104. DSP core 111 has "read" access within subsystem A 101 to unshared local RAM 112 via bus program (P) bus 130 and shared RAM 113 also via P bus 130. DSP core 111 has "write" access within subsystem A 101 to unshared local RAM 112 and shared RAM 113 via E bus 122. By way of three additional busses 124, 125, and 126, DSP core 111 also has read access to shared RAM outside subsystem A 101 in the other three subsystems B 102, C 103 and D 104. Summarizing, four of the six paths from subsystem A 101 shared memory which must be arbitrated by the DARAM4W wrapper 113 are: "read" path ~~116~~ 130 from shared memory 113 of subsystem A 101 to a DSP core of another of the three subsystems; "read" path 124 from shared memory 133 of subsystem B to DSP core 111 of subsystem A; "read" path 125 from shared memory 153 of subsystem C to DSP core 111 of subsystem A; and "read" path 126 from shared memory 173 of subsystem D to DSP core 111 of subsystem A.--

Rewrite the paragraph at page 7, line 26 to page 8, line 8 as follows:

--The global traffic module 115 decodes the address 109 of DSP P bus 130. Global traffic module 115 drives memory bank selects 117 to the four-way shared memory wrapper 127 and decodes two program address busses 109 to determine if an access is to the local block of global memory or to global memory associated with another subsystem. Because Figure 2 is describing a particular subsystem (in this case subsystem A 101), there is an additional task its global traffic module 115 must perform. Global traffic module 115 arbitrates access by signals 128 ~~two~~ of the other subsystems to a third subsystem for four-way shared program "read". Finally, it also communicates a global acknowledge signal 129 as part of its communication with DSP core 111.--

Rewrite the paragraph at page 14, line 27 to page 15, line 14 as follows:

--Figure 3 illustrates conceptually the flow of data arbitrated within a subsystem. Subsystem A 101 is used as an example. Six request inputs are shown representing the six accesses which are arbitrated. Request 314 is associated with an address "P1 Address" and request 315 is associated with an address "P3 Address". Four other similar requests can be simultaneously present at arbitration request inputs 330. Arbitration and data steering logic 304 receives these inputs and separate write data inputs from M bus 121 and E bus 122. Addresses 327 are sent to address steering logic 303. Address steering logic 303 supplies two addresses to multiplexer 326. Multiplexer 326 ~~selected~~ selects one address as controlled by strobe (STRB) signal 307. The selected address input A 317 contains the required address for each half-clock cycle switched by multiplexer 326 as driven by STRB signal 307. STRB signal 307 and inverted opposite phase signal STRBZ (which are

collectively labeled STRB 307) are derived in buffered form from the main DSP clock.--